CLAIMS

What is claimed is:

1. A self-programmable chip comprising:

a reconfigurable array processing network, providing:

(a) a feed-forward neural network; and

(b) learning modules; and

at least one control block providing digital memory and at least one control module supplying ordered signal routing functionality for said processing network.

2. The chip of claim 1, wherein the chip has a mixed-mode design.

3. The chip of claim 1, wherein the forward network and learning modules process in analog continuous-time mode, while the parameters are stored on chip in digital form.

4. The chip of claim 1, wherein said processing network includes a first interconnection structure.

5. The chip of claim 1, wherein said processing network includes a plurality of 4-quadrant multipliers operably coupled to said first interconnection structure.

6. The chip of claim 1, wherein said processing network includes a plurality of transconductance amplifiers operably coupled to said first interconnection structure.

7. The chip of claim 1, wherein said processing network includes a plurality of active load resistances operably coupled to said first interconnection structure.

8. The chip of claim 1, wherein the plurality of control blocks includes a second interconnection structure.

9. The chip of claim 1, wherein the plurality of control blocks includes a plurality of D-Flip-flops operably coupled to said second interconnection structure.

10. The chip of claim 1, wherein the plurality of control blocks includes a plurality of analog to digital converters operably coupled to said second interconnection structure.

11. The chip of claim 1, wherein the plurality of control blocks includes a plurality of multiplying digital to analog converters operably coupled to said second interconnection structure.

12. The chip of claim 1, wherein the plurality of control blocks includes a plurality of comparators operably coupled to said second interconnection structure and operable to perform parameter storage and analog to digital conversions.

13. A synaptic cell with on-chip learning and synaptic weight storage integrated therein, the synaptic cell comprising:

a communications medium operable to transmit input target data;

learning hardware operable to compute synaptic weights based on the input target data; and

a storage medium operable to store the computed weights,

wherein the synaptic cell is implemented in hardware on a single chip.

14. The synaptic cell of claim 13, wherein said communications medium comprises an interconnect data bus.

15. The synaptic cell of claim 13, wherein said learning hardware comprises a capacitor.

16. The synaptic cell of claim 13, wherein said learning hardware comprises a plurality of one-dimension multipliers.

17. The synaptic cell of claim 13 in communication with an analog to digital converter operable to convert the weights to digital form.

18. The synaptic cell of claim 13, wherein said storage medium comprises a plurality of data flip-flops operable to store the computed weights in digital form.

19. A self-programmable chip comprising:

a chip substrate providing a transmission medium;

a plurality of synaptic cells implemented on said chip substrate with on-chip learning and weight storage integrated therein; and

at least one control cell implemented on said chip substrate and operable to route signals to and from said plurality of synaptic cells in an ordered fashion.

20. The chip of claim 19, wherein at least one synaptic cell of said plurality of synaptic cells comprises learning hardware operable to compute weights based on input target data.

21. The chip of claim 20, wherein said learning hardware comprises a capacitor.

22. The chip of claim 20, wherein said learning hardware comprises a plurality of one-dimension multipliers.

23. The chip of claim 20, wherein said synaptic cell comprises an analog to digital converter operable to convert the weights to digital form.

24. The chip of claim 19, wherein at least one synaptic cell of said plurality of synaptic cells comprises a storage medium operable to store computed weights.

25. The chip of claim 24, wherein said storage medium comprises a plurality of data flip-flops operable to store the computed weights in digital form.

26. The chip of claim 19, wherein said chip substrate comprises an interconnect having a data bus.

27. The chip of claim 19, wherein said plurality of synaptic cells and a plurality of said control cells is organized into an array structure comprising identical cells of 17X16 synaptic cells augmented by a column of control cells, the chip further comprising decoders and de-multiplexers operable to provide chip level programming of synaptic weights for multiple blocks in parallel, said decoders and demultiplexers used for both row and column selections.

28. A method of operating a self-programmable chip comprising:

activating a learning mode;

activating a storage mode; and

activating a process mode.

29. The method of claim 28 further comprising activating a program mode.

30. The method of claim 29, wherein said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read out.

31. The method of claim 29, wherein said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read in.

32. The method of claim 29, wherein said activating a program mode comprises activating a program mode, wherein the chip accomplishes weight read in, wherein the weight read in signifies programming the weights for applications where the chip has already been trained.

33. The method of claim 28, wherein said activating a learning mode comprises activating a learning mode that is purely analog.

34. The method of claim 28, wherein said activating a learning mode comprises activating a learning mode, wherein the chip activates a learning process based on inputs and desired output targets supplied by at least one of an application and a user.

35. The method of claim 28, wherein said activating a storage mode comprises activating a storage mode that is analog-digital.

36. The method of claim 28, wherein said activating a storage mode comprises activating a storage mode, wherein a user, once satisfied with performance of a chip network in the learning mode, saves computed weights in on-chip static digital memory.

37. The method of claim 28, wherein said activating a storage mode comprises automatically activating a storage mode after passage of a predetermined amount of time since activation of the learning mode.

38. The method of claim 28, wherein said activating a process mode comprises activating a process mode, wherein outputs are generated by a chip forward network.

39. A method of making a self-programmable chip, comprising:

providing a chip substrate having a databus;

operably attaching a plurality of synaptic cells to the chip substrate, wherein the synaptic cells have on-chip learning and synaptic weight storage integrated therein; and

operably attaching at least one control cell to the chip substrate, wherein the control cells are operable to route signals in an ordered fashion.

40. The method of claim 39, wherein said operably attaching a plurality of synaptic cells to the chip substrate comprises:

operably attaching a capacitor to the chip substrate; and

operably attaching a plurality of one-dimension multipliers to the chip substrate in the vicinity of the capacitor; and

interconnecting the capacitor and the one dimensional multipliers in a configuration causing the plurality of the one-dimension multipliers to scale an input target signal, while the capacitor allows a voltage of the input target signal to cause a synaptic weight to settle over time.

41. The method of claim 40, wherein said operably attaching a plurality of synaptic cells to the chip substrate comprises:

operably attaching an analog to digital converter to the chip substrate in the vicinity of the capacitor, wherein the analog to digital converter is operable to convert the synaptic weight to digital form; and

operably attaching at least one data flip-flop to the chip substrate in the vicinity of the analog to digital converter, wherein the data flip-flop is operable to store the synaptic weight in digital form.

42. A programmable filter comprising:

a chip substrate providing a transmission medium;

a programmable filter structure implemented on said chip substrate and operable to receive an input signal, filter the input signal according to predetermined weights, and output the filtered signal, said programmable filter structure comprising:

(a) an input operable to receive data comprising predetermined weights;

(b) a storage medium operable to store the predetermined weights; and

(c) an output operable to communicate stored weights off chip.